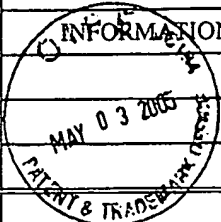
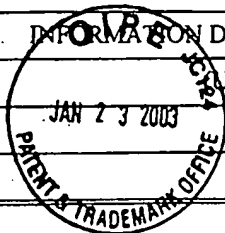


U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Application No.		
 INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute PTO Form 1449				NS-5127 US		10/054,653		
				Applicant(s)		Confirmation No.		
				Constantin Bulucea		9448		
				Filing Date		Group		
				January 18, 2002		2814		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA							
	AB							
	AC							
	AD							
	AE							
	AF							
	AG							
	AH							
	AI							
	AJ							
	AK							
Foreign Patent Documents								
		Document	Date	Country	Class	Subclass	Translation	
							Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
DR	AQ	Takeuchi et al, "A New Multiple Transistor Design Methodology for High Speed Low Power SOC's," <u>IEDM Technical Digest</u> , December 2001, pages 22.6.1 - 22.6.7						
	AR							
	AS							
Examiner <i>[Signature]</i>		Date Considered <i>9/3/05</i>						
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Application No.	
				NS-5127 US		10/054,653	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant		Confirmation No.	
(Use several sheets if necessary)				Constantin Bulucea		9448	
				Filing Date		Group	
				January 18, 2002		2814	
U.S. Patent Documents							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
DF	AA	5,399,893	03/95	Weitzel et al.	257	355	
DF	AB	5,497,028	03/96	Ikeda et al.	257	531	
DF	AC	6,100,770	08/00	Litwin et al.	331	117 FE	
DF	AD	6,166,404	12/00	Imoto et al.	257	279	
	AE						
Foreign Patent Documents							
							Translation
	Document	Date	Country	Class	Subclass	Yes	No
AF	6-61446	03/1994	Japan				X
AG							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
DF	AH	Andreani, et al., "A 1.8-GHZ CMOS VCO Tuned by an Accumulation-Mode MOS Varactor," IEEE Intl. Symposium on Circuits and Systems, 28 - 31 May 2000, pp. I-315 - I - 318.					
	AI	Grove, <u>Physics and Technology of Semiconductor Devices</u> (John Wiley & Sons), 1967, pp. 263 - 305.					
	AJ	Grove, et al., "Effect of Surface Fields on the Breakdown Voltage of Planar Silicon <i>p-n</i> Junction," <u>IEEE Trans. Electron Devices</u> , vol. ED-14, 1967, pp. 157 - 162.					
	AK	Grove, et al., "Surface Effects on <i>p-n</i> Junctions: Characteristics of Surface Space-Charge Regions Under Non-Equilibrium Conditions," <u>Solid-State Electronics</u> , Vol. 9, 1966, pp. 783 - 806.					
	AL	Kral, et al., "RF-CMOS Oscillators with Switched Tuning," <u>Procs. IEEE Custom Integrated Circuits Conference</u> , 1998, pp. 555 - 558.					
	AM	Lee, <u>The Design of CMOS Radio-Frequency Integrated Circuits</u> (Cambridge Univ. Press), 1998, pp. 37 - 41 and 504 - 514.					
	AN	McMahon, et al., "Voltage-Sensitive Semiconductor Capacitors," <u>1958 IRE Wescon Conf. Rec.</u> , Part 3, 19 - 22 August 1958, pp. 72 - 82.					
DF	AO	Moll, "Variable Capacitance With Large Capacity Change," <u>IRE Wescon Conf. Rec.</u> , Vol. 3, 1959, pp. 32 - 36.					
Examiner <i>[Signature]</i>		Date Considered 9/3/05					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Application No.		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				NS-5127 US		10/054,653		
				Applicant		Confirmation No.		
				Constantin Bulucea		9448		
				Filing Date		Group		
				January 18, 2002		2814		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA							
	AB							
	AC							
	AD							
	AE							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AF							
	AG							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
DF	AH	Ng, <u>Complete Guide to Semiconductor Devices</u> (McGraw Hill), 1995, pp. 11 - 22.						
	AI	Razavi, <u>Design of Analog CMOS Integrated Circuits</u> (McGraw Hill), 2001, pp. 495 - 525.						
	AJ	Rusu et al., "Deep-Depletion Breakdown Voltage of Silicon-Dioxide/Silicon MOS Capacitors," <u>IEEE Trans. Elec. Devs.</u> , March 1979, pp. 201 - 205.						
	AK	Rusu et al., "Reversible Breakdown Voltage Collapse in Silicon Gate-Controlled Diodes," <u>Solid-State Electronics</u> , Vol. 23, 1980, pp. 473 - 480.						
	AL	Sedra, et al., <u>Microelectronic Circuits</u> , (4th ed., Oxford Univ. Press), 1998, p. 382.						
	AM	Svelto, et al., "A Three Terminal Varactor for RF IC's in Standard CMOS Technology," <u>IEEE Transactions on Electron Devices</u> , Vol. 47, 2000, pp. 893 - 895.						
	AN	Warner, Jr., et al., <u>Transistors - Fundamentals for the Integrated-Circuit Engineer</u> (John Wiley & Sons), 1983, pp. 320 - 321.						
DF	AO	Wong et al., "A Wide Tuning Range Gated Varactor," <u>IEEE J. Solid State Circs</u> , May 2000, pp. 773 - 779.						
Examiner		Date Considered						
		9/3/05						
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								